REMARKS

The rejection of claim 1 based on Solheim seems to rely on the principle that the teaching of the general can be relied upon to anticipate the specific. As a proposition of law and logic, the position is untenable.

For example, teaching that anything can be done or that something can be done without teaching the specifics or the specific way claimed is insufficient to meet the claimed limitations. The office action suggests that Figure 3 teaches converting between DS3 in Sonet in Figure 3, but nothing in the patent itself seems to support this proposition. Nor is it clear that such a conversion would involve using a register, writing blocks of demultiplexed data at a first size into the register, and reading blocks of a second size different from the first size from the register. For example, even if DS3 and Sonet conversions require changing of block sizes, there is no reason to presume, nor is it inherent, that it would be done in the claimed way. There is certainly much more elaborate ways that the block size could be converted and there is no basis to presume that even if Solheim in general taught an embodiment in which block size must have been converted, that he did it in the way claimed.

It is contended that the rejection relies on too generic teachings in the reference because everything that is cited is general and is not specific to what is claimed. For example, the material in paragraph 7 of the office action is very general. The citation of paragraph 30, lines 1-4, is so general as to be non-informing. Column 30, lines 1-4 simply says "The mapping device 110, after inputting the buffered data information BD1, BD2 from the buffering devices 106, 108 maps its data information in data units consistent with a particular format." Whatever this means, it certainly is not specific to converting block size in the way claimed. The same may be said in the material in paragraphs 51 and 71. None of these talk about converting block size, be it packet or frame size, or any other unit of data. And, most certainly, it does not teach doing so by writing the blocks at a first size into a register and reading the blocks at a second size from the register. Thus, reconsideration would be appropriate.

The same arguments apply to claim 11. With respect claims 12 and 13, these were rejected over Solheim in view of Song. The rejection states that Song teaches all aspects of the claimed invention as set forth in the rejections of claim 11 "but fails to teach a device including a first counter to control the writing of data from the demultiplexer to the register and a second counter to

control the reading of data from the register to the multiplexer." Thus, the reason for citing Song is unclear.

Claim 23 calls for examining a window to determine whether at least one synchronization bit is located within data within a window of predetermined size within a data stream. The window is shifted along the stream if a valid synchronization bit is not found in the window 32. Claim 31 calls for providing serial data a first array of multiplexers arranged in rows and columns, wherein each row corresponds to a different window position along the stream of data. In response to this claim element, it is asserted that Iwanczuk discloses an array of multiplexers in detecting synchronization patterns. But even if this is true, it hardly reaches the claimed subject matter.

Therefore, reconsideration of the rejection of claims 31 and 32 is respectfully requested.

On a similar basis, reconsideration of the rejections of claims 44-55 is respectfully requested.

With respect to claim 44, nothing in Figure 9 appears to show multiplexers arranged in rows and columns. Nor there is anything that teaches a row of multiplexers providing one window of data as set forth in claim 45 or a second array of multiplexers coupled to the first array as set forth in claim 46.

In view of these remarks, reconsideration is respectfully requested.

Respectfully submitted,

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